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... in using Protocol Compiler in a ATM ASIC project.", **SNUG**'99, Munich ... Programmable Logic and System-Level ICs", Atmel Corporation, **San Jose**, May **2000**. ...

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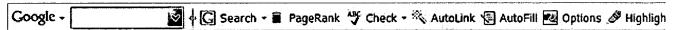
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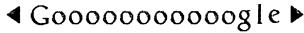
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